REMARKS

Claims 25-34 are currently pending in the above-identified application. Claims 1-24 and 35-38 have been canceled without prejudice or disclaimer to the subject matter recited therein and solely for the purpose of furthering the prosecution of this application. Applicants reserve the right to claim the subject matter of the canceled claims and other claims in this or any other application. Claims 25, 30 and 34 have been amended.

The specification and claims are objected to as being informal. Applicants submit that appropriate correction has been made; the application as amended is in proper form.

Claims 25-34 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Reconsideration is respectfully requested. Applicants have amended claim 25, which now incorporates former claim 24, to state --said dielectric substrate--.

Claim 34 are rejected under 35 U.S.C. § 102 as being anticipated by Heo. Reconsideration is respectfully requested. Claim 34 depends from amended claim 25 and incorporates by reference the limitations of original claim 24. Applicant respectfully submits that Heo fails to disclose or suggest the limitations of original claim 25 in combination with original claim 24. Therefore, for at least this reason, the rejection of claim 34 should be withdrawn.

Claims 25-33 are rejected under 35 U.S.C. § 102 as being anticipated by Marcantonio. Reconsideration is respectfully requested. The present invention is directed to packaging for semiconductor devices wherein the package comprises, among others, a metal layer formed between a semiconductor layer and a dielectric substrate. A package having this configuration provides beneficial characteristics. For example, in a

package 60, a metal layer 62 is provided between the semiconductor device 12 and substrate 14, the substrate 14 being laminated to the metal layer 62. Consequently, the stiffness of package 60 is improved. See page 8, lines 1-3 of the Applicant's specification; Figure 4.

Accordingly, amended claim 25 now recites a "a metal layer formed between said semiconductor layer and said dielectric substrate." This is an important feature of the invention. Marcantonio does not teach or suggest the metal layer of the claimed invention. Rather, Marcantonio provides a "heat spreader" 214 which is disposed on a side opposite to that of both the integrated circuit chip 212 and the dielectric layers 224, 226, 228 (col. 4, lines 41-67). Thus, it appears that Marcantonio would suffer from the same drawbacks of the prior art as described in Applicant's specification on page 2, namely, a package without sufficient stiffness. Claims 26-34 should be allowable along with claim 25 and for other reasons.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Referring now to the drawings, where like reference numerals designate like elements, there is shown in FIG. 1 a semiconductor device package 10 constructed in accordance with one embodiment of the present invention. The package 10 has a semiconductor device 12, a dielectric substrate 14, and a ball grid array (BGA) 16. The semiconductor device 12 has an integrated circuit (not shown). A suitable adhesive 18 may be used to secure the semiconductor device 12 to the substrate 14. The semiconductor device 12 and the substrate 14 may be diced from a layered wafer-tape assembly 20 as described in more detail below in connection with FIG. 2. The dicing process causes [the] edges 22 of the substrate 14 to be aligned with [the] edges 24 of the semiconductor device 12.

The ball grid array 16 may be used to mechanically and electrically connect the package 10 to a circuit board (not shown). Wire bonds 26, bond pads 28, circuit traces 30, and ball pads 32 may be used to provide electrical communication between the semiconductor device 12 and the ball grid array 16. The wire bonds 26 extend through a slot-shaped opening 34. The traces 30 may be printed on [the] a top surface 36 of the substrate 14 (before the semiconductor device 12 is adhered to the substrate 14). An insulative solder mask 38 extends over the traces 30. The mask 38 has openings 40 for receiving the individual balls of the ball grid array 16. A screen printing process may be used to apply the solder mask 38 as a paste to the entire surface of the substrate 14 except for the slot-shaped opening 34 and the ball pads 32. The wire bonds 26 and the bond pads 28 may be encapsulated in a suitable liquid encapsulant 42.

The package 60 may be singulated from a wafer-tape assembly of the type shown in FIGS. 2 and 3. With respect to the FIG. 4 embodiment, however, a metal sheet (not shown) is located between the wafer 50 and the tape 52 before the dicing operation. The metal layer 62 is singulated from the metal sheet when the assembly is

diced (after full wafer testing). The metal sheet may cover all of the semiconductor devices 12 in the wafer 50. The dicing operation causes [the] edges 64 of the metal layer 62 to be aligned with [the] edges 22, 24 of the substrate 14 and the semiconductor device 12. As in the embodiment of FIGS. 1-3, plural packages 60 may be tested and burned-in before they are singulated from the layered assembly.

As shown in FIG. 6, a solder mask 82 extends over the exterior traces 78. The mask 82 has openings 40 aligned with the ball pads 32 for receiving the solder balls and/or conductive bumps of the ball grid array 16. The mask 82 extends all the way across the central portion 84 of the substrate 72. Similarly to the FIGS. 1-5 embodiments, the package 70 shown in FIG. 6 may be singulated from a wafer-tape assembly. That is, the substrate 72 may be diced from a larger sheet of dielectric material (not shown) after the sheet is attached to a wafer 50, and after all of the packages 70 are tested and burned-in. The dicing operation causes [the] edges 24 of the semiconductor device 12 to be aligned with [the] edges 86 of the substrate 72.

If desired, a metal layer 90 (FIG. 7) may be attached to the semiconductor device 12 by a suitable adhesive 92. The thickness of the metal layer 90 may be in the range of from about 0.13 millimeters to about 0.25 millimeters. The metal layer 90 may operate as a heat sink or heat spreader to thermally stabilize the semiconductor device 12. In addition, the metal layer 90 may provide stiffness for [the] package 94. The metal layer 90 is preferably attached to the semiconductor device 12 before the device 12 is singulated from the wafer 50. This way, the metal layer 90 provides stiffness to the wafer-tape assembly prior to and during the dicing operation. The dicing operation causes [the] edges 96 of the metal layer 90 to be aligned with [the] edges 24, 86 of the semiconductor device 12 and the substrate 72.

25. (Amended) [The package of claim 24, further comprising a metal layer having edges formed by said dicing operation.] A semiconductor device package, comprising:

a semiconductor device having edges formed by a dicing operation;

a dielectric substrate having edges formed by said dicing operation;

a metal layer formed between said semiconductor device and said dielectric substrate having edges formed by said dicing operation;

a ball grid array on said dielectric substrate, said dielectric substrate and said metal layer being located between said semiconductor device and said ball grid array; and

electrical connections between said semiconductor device and said ball grid array.

30. (Amended) The package of claim 25, wherein said connections [e] comprise wire bonds.

34. (Amended) The package of claim [24] 25, further comprising an insulative solder mask for covering said dielectric substrate.